This listing of claims will replace all prior versions, and listing, of claims in the application:

Listing of Claims:

1. (previously amended) An integrated circuit for a digital still camera for performing image pipeline tasks, comprising:

(a) a first programmable processor programmed to run control functions, said first processor coupled to a user interface, a controller for memory, and a controller for image acquisition;

(b) a second programmable processor programmed to run image processing and compression functions, said second processor coupled to said first processor; and

(c) a third processor coupled to said second processor, said third processor including ~~at least four~~ more than one parallel multiply and accumulate units, wherein the integrated circuit utilizes parameter-driven address generation and looping control.

2. (canceled)

3. (currently amended) An integrated circuit for a digital still camera, comprising:

(a) a first programmable processor programmed to run control functions, said first processor coupled to a user interface, a controller for memory, and a controller for image acquisition;

(b) a second programmable processor programmed to run image processing and compression functions, said second processor coupled to said first processor; and

(c) an image compression unit separate from said second processor, said compression unit arranged to compress acquired images for storage in a memory and to decompress said compressed acquired images in said memory for restorage in said memory, wherein the integrated circuit utilizes parameter-driven address generation and looping control.

4. (currently amended) An integrated circuit for a digital still camera, comprising:

(a) a first programmable processor programmed to run control functions, said first processor coupled to a user interface, a controller for memory, and a controller for image acquisition;

(b) a second programmable processor programmed to run image processing and compression functions, said second processor coupled to said first processor; and

(c) a digital image processing unit separate from said first and second processors, said image processing unit arranged for real-time image sequence (video) processing, said image processing unit controlled in real-time by said first processor wherein the integrated circuit utilizes parameter-driven address generation and looping control.

5. (currently amended) The integrated circuit of claim 1, further comprising:

~~(a)~~ (d) an audio input coupled to said second processor, said second processor programmed to decode audio and said first processor programmed to output said decoded audio.

6. (currently amended) The integrated circuit of claim 1, further comprising:

~~(a)~~ (d) camera peripherals including IfSA, USB, NTSC/PAL encoder, and compact flash/smart media interface.